REMARKS

Claims 2-21 were pending in this application.

Claims 2-5 and 12-15 have been rejected.

Claims 6-11 and 16-19 have been objected to.

Claims 20-21 have been allowed.

Claims 5 and 15 have been amended as shown above.

Claims 2-21 remain pending in this application.

Reconsideration and full allowance of Claims 2-21 are respectfully requested.

I. ALLOWABLE CLAIMS

The Applicant thanks the Examiner for the indication that Claims 20-21 are allowable. Claims 20-21 have not been amended and therefore remain in condition for allowance.

The Applicant also thanks the Examiner for the indication that Claims 6-11 and 16-19 would be allowable if rewritten in independent form. Because the Applicant believes that the remaining claims in this application are allowable, the Applicant has not rewritten Claims 6-11 and 16-19 in independent form.

II. INITIAL MATTERS

First, Claims 2 and 12 recite that an "instruction that loads data from a first memory location that was previously stored to" is detected "without requiring computation of an external memory address of said first memory location." The Applicant respectfully notes that Claims 2

and 12 should be interpreted as they are written. To the extent that the Patent Office attempts to read a time period when the "external memory address" is not computed into Claims 2 and 12, this is inappropriate. Moreover, to the extent that the Patent Office interprets terms in Claims 2 and 12 that are inconsistent with or different from the specification, this is also inappropriate. Claims 2 and 12 should be interpreted and examined based on their actual recitations – an "instruction that loads data from a first memory location that was previously stored to" is detected "without requiring computation of an external memory address of said first memory location."

Second, the Office Action allegedly identifies an ambiguity in Claims 2 and 12, stating that it is unclear whether the Applicant is "claiming the detection of the load instruction itself without requiring the computation" or is "claiming the detection of the load instruction in addition to the 'without computation.'" (*Office Action, Page 2, Paragraph 7*). Claims 2 and 12 clearly recite that an "instruction that loads data from a first memory location that was previously stored to" is detected "without requiring computation of an external memory address of said first memory location." There is no ambiguity here – the instruction is detected without requiring that the external memory address be computed.

Third, the Office Action states that the originally filed application may lack written description or an enabling disclosure for these recitations in Claims 2 and 12. However, the application as originally filed clearly recites "detecting instructions ... without having to actually compute the referenced external memory addresses." (*Application, Page 4, Lines 8-11*). The application as originally filed then describes at least one technique for detecting instructions

without computing the referenced external memory addresses. (*Application, Page 4, Lines 11-16*). For example, the application as originally filed clearly recites how a "bypass element 121" operates and detects instructions without requiring that the "external memory address" of the instructions be computed. (*Application, Page 8, Line 20 – Page 9, Line 7*). Based on this, the Applicant respectfully submits that the application as originally filed complies with the written description and enablement requirements.

III. REJECTION UNDER 35 U.S.C. § 102

The Office Action rejects Claims 2-5 and 12-15 under 35 U.S.C. § 102(a) or § 102(b) as being anticipated by U.S. Patent No. 5,475,823 to Amerson et al. ("*Amerson*"). This rejection is respectfully traversed.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. (*MPEP § 2131; In re Bond, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990)*). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. (*MPEP § 2131; In re Donohue, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985)*).

The Office Action asserts that *Amerson* discloses a system for "determining the same address by comparing the partial or complete address referenced by the load instruction with the store address." (*Office Action, Page 5, Paragraph 16*). The Office Action also asserts that the comparison "was done based on the overlapping of the partial memory address, therefore, no

calculation of the actual effective address was needed." (*Office Action, Page 5, Paragraph 16*). The Office Action cites column 8, lines 13-54 of *Amerson* as supporting these assertions. (*Office Action, Page 5, Paragraph 16*).

The cited portion of *Amerson* does not recite that a "partial address" or a "complete address" in a load instruction is compared to the address of a store instruction. The cited portion of *Amerson* actually recites that the "addresses of all store instructions" are compared to the "addresses of the load instructions" in a register file. (*Col. 8, Lines 29-31*). This is done to "check for partial or complete overlap of the memory locations accessed by the load and store instructions." (*Col. 8, Lines 31-33*).

This portion of *Amerson* lacks any mention of comparing "partial" addresses or "complete" addresses. Instead, this portion of *Amerson* clearly states that the "addresses" of load and store instructions are compared. This portion of *Amerson* also clearly states that this function is performed to determine if a load instruction refers to memory addresses that partially or completely overlap memory addresses referred to in a store instruction.

Moreover, it is irrelevant whether *Amerson* compares "partial" or "complete" memory addresses. The only issue is whether *Amerson* is required to compute an external memory address in order to operate. The Office Action has failed to show that *Amerson* detects an instruction that loads data from a memory location previously stored to "without requiring computation of an external memory address" of the memory location. In fact, as noted above, *Amerson* clearly recites that the "addresses" of the load and store instructions are used and compared in order to detect an instruction. This clearly shows that *Amerson* is required to

compute external memory addresses in order to operate.

For these reasons, the Office Action fails to show that *Amerson* anticipates the Applicant's invention as recited in Claims 2 and 12 (and their dependent claims). Accordingly, the Applicant respectfully requests withdrawal of the § 102 rejection and full allowance of Claims 2-5 and 12-15.

IV. REJECTION UNDER 35 U.S.C. § 103

The Office Action rejects Claims 2-5 and 12-15 under 35 U.S.C. § 103(a) as being unpatentable over *Amerson* in view of U.S. Patent No. 6,360,314 to Webb, Jr. et al. ("*Webb*"). This rejection is respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. (*MPEP § 2142; In re Fritch, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992)*). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984)*). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993)*). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. (*In re Oetiker, 977 F.2d 1443,*

1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Grabiak, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985)).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. (*In re Bell, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993)*). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. (*MPEP § 2142*).

The Office Action asserts that *Webb* discloses a "bypass circuit for comparing the address of a load with the address of a recent store, and if match occurs the store provided the data instead of retrieving data from the memory." (*Office Action, Page 6, Paragraph 17*). The Office Action also asserts that "no calculation of the actual effective address to the memory was needed because the retrieval from the memory was avoided." (*Office Action, Page 6, Paragraph 17*).

The Office Action cites no support for its assertion that the "actual effective address" in *Webb* is not calculated because a "retrieval from the memory was avoided." In effect, the Office Action is assuming that the "actual effective address" is never calculated if data is not retrieved from memory. This assumption has no support in *Webb*. In fact, this assumption is expressly

contradicted in *Webb*.

Webb clearly recites that the physical address of a memory location is used by the system. In particular, "bits 43:13" of the physical address are used by the system of *Webb*. (*Col. 6, Lines 3-17*). Based on these bits of the physical address, a fetch to external memory may or may not occur. (*Col. 6, Lines 3-17*).

It is clear here that *Webb* uses the actual physical address for a load operation to determine whether to fetch data from external memory. Because of this, the Office Action cannot assume that the "actual effective address" of a load instruction is not calculated because "the retrieval from the memory was avoided."

Moreover, this portion of *Webb* clearly recites that the external memory address is used to determine if a load instruction is loading data to a location that was previously stored to. As a result, this portion of *Webb* clearly fails to disclose, teach, or suggest detecting an "instruction that loads data from a first memory location that was previously stored to" without "requiring computation of an external memory address of said first memory location" as recited in Claims 2 and 12.

For these reasons, the proposed *Amerson-Webb* combination fails to disclose, teach, or suggest the Applicant's invention as recited in Claims 2 and 12 (and their dependent claims). Accordingly, the Applicant respectfully requests withdrawal of the § 103 rejection and full allowance of Claims 2-5 and 12-15.

V. CONCLUSION

As a result of the foregoing, the Applicant asserts that all pending claims in the application are in condition for allowance and respectfully requests an early allowance of such claims.

SUMMARY

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication (including any extension of time fees) or credit any overpayment to Davis Munck Deposit Account No. 50-0208.

Respectfully submitted,

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